AREA EFFICIENT MULTILAYER ARITHMETIC LOGIC UNIT IMPLEMENTATION IN QUANTUM-DOT CELLULAR AUTOMATA

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ABSTRACT:

Quantum-dot Cellular Automata (QCA) is a new nano-scale technology that due to making significant improvements in the design of electronic circuits can be considered as an appropriate alternative to CMOS technology. The Arithmetic Logic Unit (ALU) is a fundamental component of the Central Processing Unit (CPU) to carry out the arithmetic and logical operations that multiplexer and full adder play an important role in its operations. In this paper, based on the extracted features of the arithmetic operations of the ALU, we propose a new special low-complexity QCA 2:1 multiplexer, which is application-specific to the proposed ALU. Moreover, a new QCA full adder is proposed based on the cell interaction. Likewise, a QCA multilayer ALU structure is designed based on the validated proposed structures to carry out four logical and eight arithmetic operations. The functional correctness of the proposed structures are evaluated by QCA Designer tool as an accurate power estimator tool is applied to investigate their power dissipation. The simulation results demonstrate that the proposed structures outperform in comparison to counterpart designs in terms of cell number, area, latency, and power consumption.

Keywords: ALU, QCA, CPU, CMOS, Nano scale.

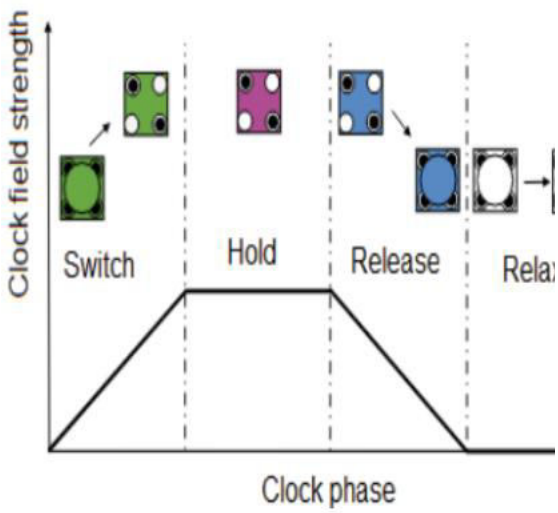
INTRODUCTION

Due to the limitations of the conventional CMOS technology, researchers extremely felt the need to find an alternative technology for the coming future. As a result, quantum-dot cellular automata (QCA) was found to be a suitable replacement that would provide unique eminent features such as small feature size at an ultra low power consumption that can operate in room temperature at a frequency range of THz [1]. The International Technology Roadmap for Semiconductors (ITRS) report lists out several nano-electronics substitutes: Single Electron Tunneling(SET), Resonant Tunneling Diodes(RTD), Tunneling Phase Logic(TPL), Quantum Dot Cellular Automata(QCA). Accordingly, QCA is

a promising technology which provides high device density at low power [2]. Further, VLSI circuits carries following limitations: power dissipation, interconnections and short channel effects. Increment in the device density within a stipulated area may result in chip damage due to the thermal effect developed over the chip. QCA is a good alternative to the silicon based technology. Advantages of QCA based systems are high speed, high device density at low power consumption. Also high parallel processing can be attained by using QCA [3].

QCA are one of those unique technologies that are considered to be smart and effective replacements for CMOS technologies. This technology can be used to design nanoscale devices with ultra compaction density capable of carrying out computations at ultra- high switching speeds of the order of GHz. QCA is transistorless computational prototype which can be used to attain device densities of (1010-1012) devices per centimeter square, while its circuit operating speed approaches (GHz-THz). It substitutes Field Effect Transistor (FET) created logic and exploits the quantum effects of very small size. QCA is a mean of representing binary logic data on cells, whereby no current flows, and better device performance is achieved by the coupling of different cells. The implementation of digital circuits in QCA is carried out by quantum cells. Each individual cell encompasses four quantum dots as two electrons. These quantum dots are nanoscale structures which are fabricated using semiconductors such as GaAs and InAs [2]. Exchange of data is accomplished by transmission of a polarized state instead of current in QCA implementation.

The quantum cell is the key module in the block diagram of that entails four quantum dots. One electron is hold by each dot. Electrostatic repulsions amongst any two electrons in the quantum cell make sure that the electrons can only exist in the anti-podal sites. Hence these electrons adopt stable states, called polarizations, which are equal and inferred as binary “1”and “0” states. It has corresponding polarizations such as =”+1” (logic “0”) and as “-1” (logic “0”).



LITERATURE SURVEY

Quantum-Dot Cellular Automata in Designing the Arithmetic and Logic Unit: Systematic Literature Review, Classification and Current Trends

Quantum-dot Cellular Automata (QCA) presents a new model at Nano-scale for possible substitution of conventional Complementary Metal–Oxide–Semiconductor (CMOS) technology. On the other hand, an Arithmetic Logic Unit (ALU) is a digital electronic circuit which performs arithmetic and bitwise logical operations on integer binary numbers. Therefore, QCA-based ALU is an important part of the processor in order to develop a full capability processor. Although the QCA has become very important, there is not any comprehensive and systematic work on studying and analyzing its important techniques in the field of ALU design. This paper provides the comprehensive, systematic and detailed study and survey of the state-of-the-art techniques and mechanisms in the field of QCA-based ALU designing. There are three categories in which QCA plays a role: ALU, logic unit (LU) and arithmetic unit (AU). Each category presents the important studies. In addition, this paper reviews the major developments in these three categories and it plans the new challenges. Furthermore, it provides the identification of open issues and guidelines for future research. Also, a Systematic Literature Review (SLR) on QCA-based ALU, LU and AU is discussed in this paper. We identified 1,960 papers, which are reduced to 26 primary studies through our paper selection process. According to the obtained results from 2001 to 2015, the number of published articles are very high in 2014 and low in 2005 and 2009. This survey paper also provides a discussion of considered mechanisms in terms of ALU, LU and AU attribute as well as directions for future research.

Design and Optimization of Reversible Multiplier CircuitDr. Rangaraju H G

The development of conventional computing technologies faces many challenges for the last couple of decades. Power dissipation in today's computer chips becomes dominant. Reversible computing is a promising alternative to

these technologies, with applications in ultra-low power, nano computing, quantum computing, low power CMOS design, optical information processing, bioinformatics etc. In reversible logic the power dissipation can be minimized or even eliminated. In this paper, the 4x4 reversible multiplier circuit is proposed with the design of new reversible gate called RAM gate. The proposed multiplier circuit is efficient compared to the existing designs in terms of gate counts, garbage outputs, constant inputs and quantum cost. The design can be generalized to construct nxn

Reversible Logic Based Arithmetic and Logic Unit.2014 •ijesrt journal

Reversible logic has received great attention in the recent years due to its ability to reduce the power dissipation which is the main requirement in low power digital design. It has wide applications in advanced computing, low power CMOS design, Optical information processing, DNA computing, bio information, quantum computation and nanotechnology. Conventional digital circuits dissipate a significant amount of energy because bits of information are erased during the logic operations. Thus, if logic gates are designed such that the information bits are not destroyed, the power consumption can be reduced dramatically. The information bits are not lost in case of a reversible computation. This has led to the development of reversible gates.

EXISTING SYSTEM

CMOS technology has some problems such as a large occupied area, short channel effects, high power dissipation, low speed, leakage currents, etc.. We have now reached the point where Moore's Law is on the verge of being limited, and thus it is not easy to increase the number of transistors due to the limitations of the manufacturing technology, an alternative technology to implement integrated circuits seems essential. Recently, a lot of studies have tried to find a suitable alternative to CMOS technology One of the proposed technologies is QCA technology QCA is a new technology used for implementing circuits at a Nanoscale. In this technology, information is transmitted between charges through Columbus interaction. Moreover, a quantum cell is the basic computational element in QCA. Besides, an inverter (NOT) gate and a three-input majority gate (MV3) are two important structures in this technology. Due to the lack of electrical currents, the circuits have low power dissipation,

high speed, low occupied area, and high density

ALU is a combined digital circuit that performs computational and logical operations on binary data [7]. An ALU is a basic unit in a variety of computing circuits, including computer CPUs, floating-point units (FPUs), and GPUs, and even a single CPU, FPU, or GPU may contain several ALUs [28]. An ALU is one of the most important components in many computer circuits, so its implementation is very important in any technology, including QCA Therefore, optimizing the complexity and improving the input-to-output delay and the occupied area is very valuable

PROPOSED SYSTEM

The method presented in [9], utilizes a full adder with minimum number of cell count by using a five-input majority gate. Basically, an adder is used in many applications like arithmetic logic circuits, image processing and digital signal processing domains.

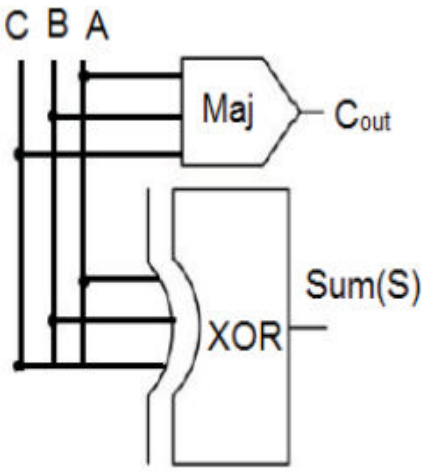


Fig 2: Logic diagram of Full adder

The full-adder is a three-input combinational circuit that computes the addition of the two digits and another bit (Cin) received from the previous adder circuit. It produces Sum (S) and Carry Out (Cout). Using K-map, the Carry Out and Sum can be calculated by Eqn. 1 and Eqn. 2, respectively. M, represents the majority gate.

$$carry\ out = ab + bc + ca = M(a, b, c) \quad (1)$$

$$sum = a \oplus b \oplus c \quad (2)$$

In the proposed adder circuit, Sum data is generated based on the categorical interfaces between the inner QCA cells, and Carry data is produced based on the majority voter. The proposed full adder as presented in Fig.2, comprises majority gate logic and three-input XOR gate. The structure can be implemented in a single layer and it has 26 cells as presented in Fig 3.

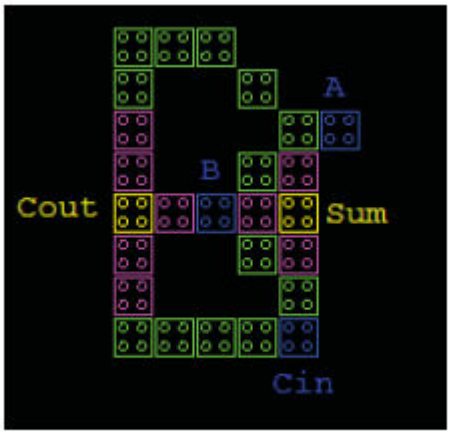


Fig 3: QCA layout of Full adder

Fig. 4, represents the application specific 4:1 multiplexer which is specially designed to implement the 1-bit ALU to perform arithmetic operations for the selection for different inputs.

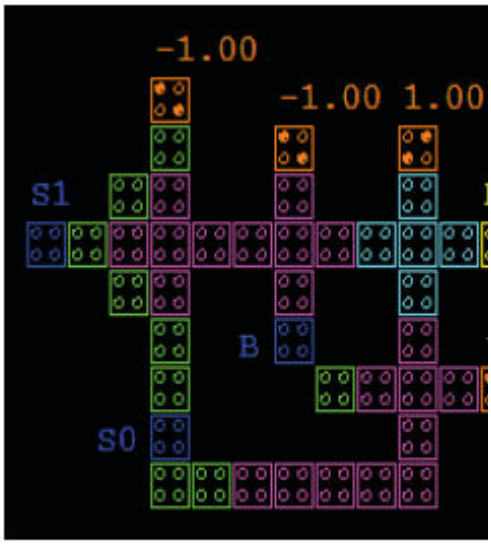


Fig. 4: QCA layout of specific 4:1 multiplexe

IMPLEMENTATION OF THE 1-BIT ALU USING 2:1 MUX

In existing designs, an application specific 1-bit ALU with 4:1 multiplier was designed which will consists of more number of cell count. To decrease the cell count a novel application specific 2:1 multiplexer with less number of cell count is proposed which is shown in below

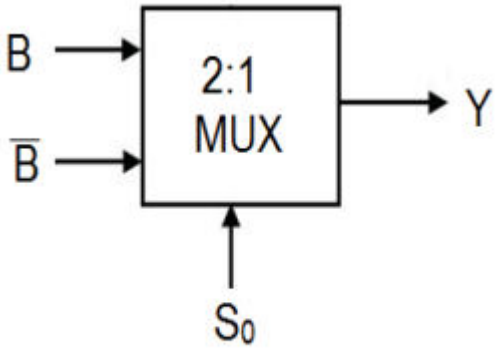


Fig. 5: Application specific 2:1 multiplier

In a 2:1 multiplexer the inputs I0 and I1 are replaced with B and as shown in below equations 3 and 4.

$$Y = \bar{S}_0 B + S_0 \bar{B} \qquad (3)$$

$$Y = S_0 \oplus B \qquad (4)$$

Using the equations 3 and 4, the 2:1 multiplexer and its QCA layout is shown

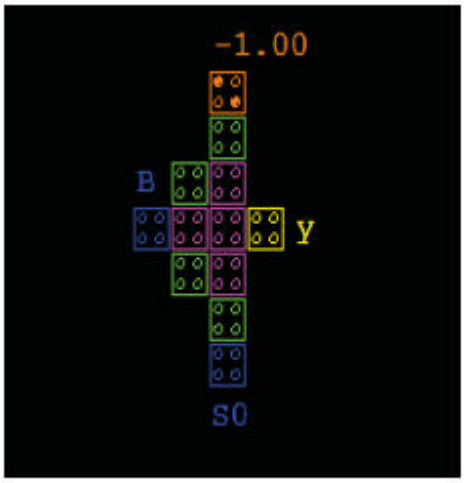
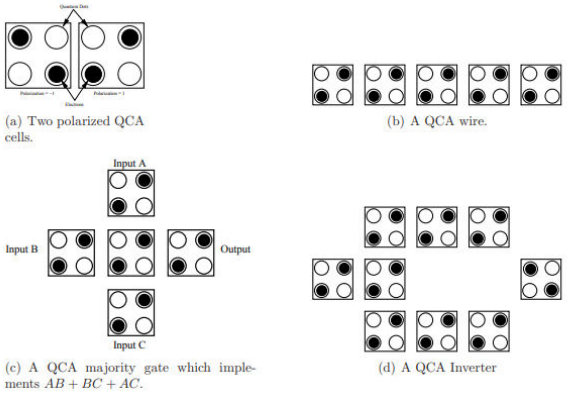


Fig.6: Application specific 2:1 multiplexer QCA layout

In this chapter QCA simulators have been discussed. The chapter begin with the very brief history of QCA simulators together with a very brief overview of

existing simulator. Next, the architectural simulation rules that comprise the engine of the simulator as well as their development will be discussed. Additionally, more detail is provided about the usage of data structures and how values propagate and change in simulations, etc. Further, a comparison of simple propagation simulators with a version of the simulator that allows addition of clocking zones is given as well. The chapter concludes with the discussion about the specific difficulties encountered when designing the circuits with the QCA simulator

In quantum-dot cellular automata (QCA), four quantum dots occupy the corners of a square cell with potential barriers between pairs of dots. Within this cell, two extra electrons are available, and by raising and lowering the potential barriers with the clock, an electron can localize on a dot. Due to Coulombic interaction, these electrons will tend to occupy antipodal sites in the square cell. Thus , two different polarizations are available: P = 1 and P = -1 as shown in Fig. 2.1(a). Respectively, these polarizations provide a logical one and a logical zero, which maintains the binary computing paradigm of the last sixty years. As Fig. 2.1(b) shows, placing several of these cells placed side by side forms a wire. Logic values then pass from cell to cell due to the Coulombic interactions. By placing groups of cells together in different configurations, logic gates can be constructed. The majority gate in Fig. 2.1(c) is the fundamental gate used in QCA, and implements the voting logic function AB + BC + AC. Holding

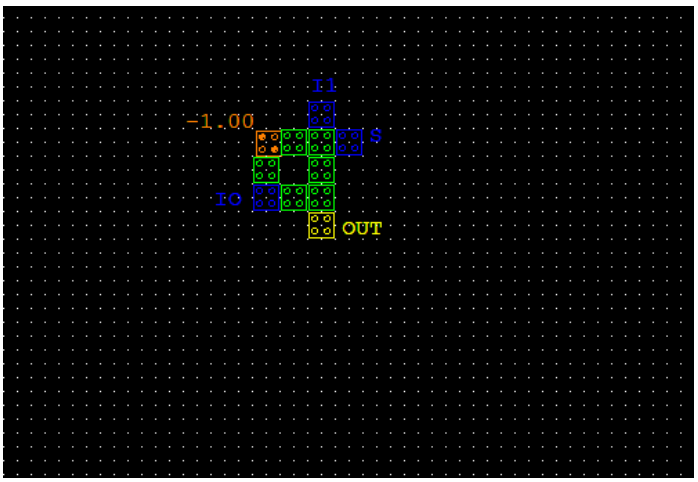


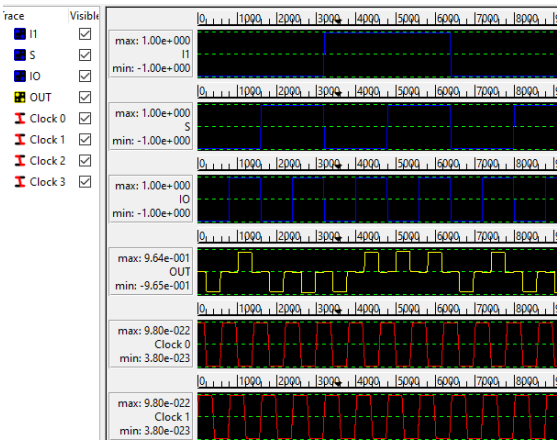
(a) Two polarized QCA cells. (b) A QCA wire. (c) A QCA majority gate which implements $AB + BC + AC$. (d) A QCA Inverter

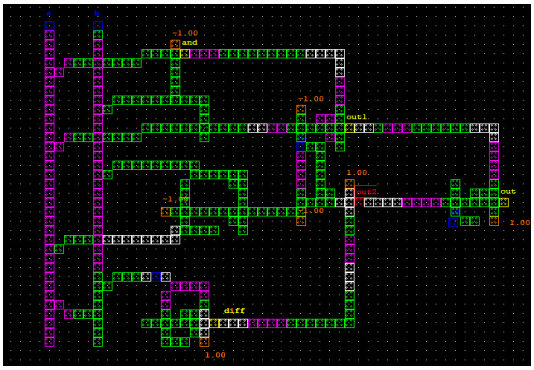
Figure 2.1. Basic QCA logic devices.

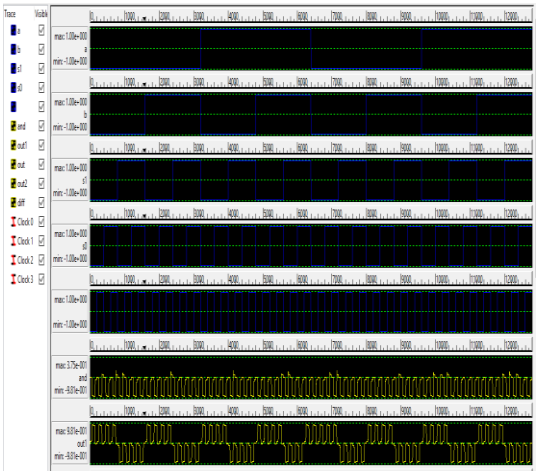
SIMULATION RESULTS:

2:1 MUX

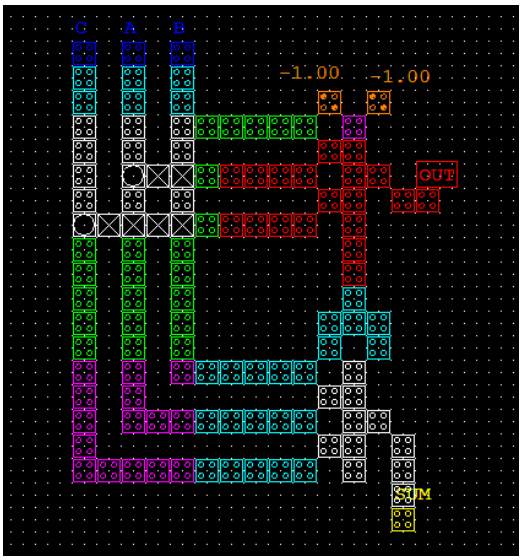


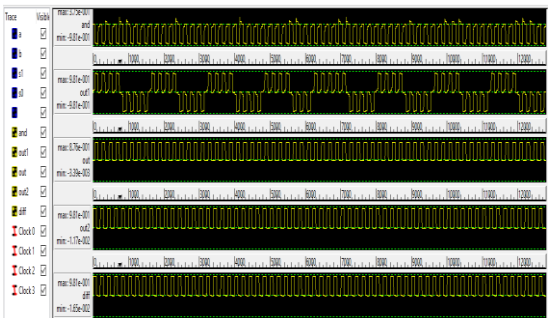


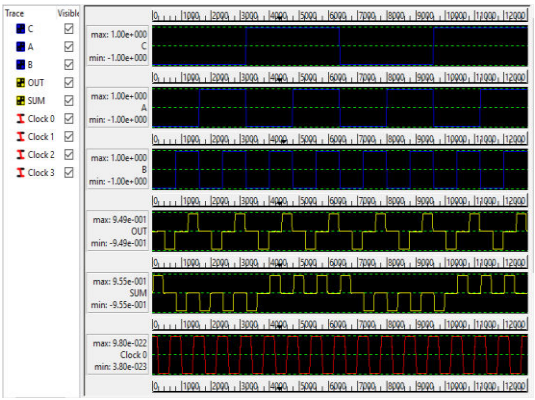




Full adder







ALU DESIGN

CONCLUSION

In this proposed work, a novel multilayer 1-bit arithmetic logic unit structure has been designed to carry out the various arithmetic and logical operations. In addition, to reduce the area overhead, the 1-bit ALU design is implemented in a multilayer. Hence these designs are implemented in one bit ALU and simulated results are verified using the QCA designer simulation tool. The multilayer 1-bit ALU design

proposed in this paper, operates with less delay and occupies less area than the previous designs

FUTURE SCOPE

In this project we are implemented 4;1 Mux using Alu designed and now in the future we can implement in processors and as well communication systems

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